

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appln. No: 10/552,429  
Applicant: David T. Beatson et al.  
Filed: August 17, 2006  
Title: ELECTRICAL INTERCONNECT STRUCTURES FOR INTEGRATED CIRCUITS AND METHODS OF MANUFACTURING THE SAME  
TC/A.U.: 1734  
Examiner: James D. Sells  
Confirmation No.: 4419  
Docket No.: KSI-323US

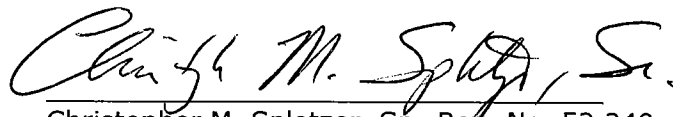
**COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE**

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.104(e), to the extent that the Examiner's Statement of Reasons for Allowance might be construed in any way to limit the scope of the allowed claims, the applicants respectfully disagree with that Statement. Specifically, for example, it is not necessary to identify any particular claim limitation as absent from the prior art for a claim to recite patentable subject matter. Most, if not all, patentable inventions are necessarily combinations of elements.

Respectfully submitted,



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Dated: September 26, 2007

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The Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **50-3643** of any fees associated with this communication.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (571)273-2885 on the date shown below.

September 26, 2007



Marjorie Poumaroux